IN THE CLAIMS:

Please **amend claim 1** as follows:

1. (*Currently amended*) A content addressable memory comprising a CAM control logic unit and a plurality of cells connected in a chain, ~~each cell comprising~~ the cells being serially connected, each of the cells including:

a memory block coupled to a common address bus;

a comparator coupled to a common data bus and to the data interface of the memory block;

a switch for coupling the data interface of the memory block with the data bus**[[,]]**; and**[[;]]**

a logic block including a Match flip-flop**[[:]]**;

the memory being operable:

in a Search phase, to serially match a sequence of words on the common data bus with the contents of a sequence of addresses in the memory blocks of the cells, the logic block being arranged for cumulatively storing the results of the matching as the matching proceeds; and

in an Access phase, to render the cells matched in the Search phase serially available for access via the common address and data buses, said Access phase occurring subsequent to said Search phase.

2. (*Previously presented*) A content addressable memory according to claim **1** wherein each cell includes a memory block, a logic block, a comparator, and a bidirectional switch.

3. (*Previously presented*) A content addressable memory according to claim **1** wherein an integrated circuit chip carries the CAM and plural cells.

4. (*Previously presented*) A content addressable memory according to claim **3** wherein several of the chips are chained.

5. (*Original*) A content addressable memory according to claim **4** wherein each chip includes a control unit which can be disabled.

6. (*Previously presented*) A content addressable memory according to claim **1** including a MASK bus input for determining which bits of the words of the sequence of words are used for matching in the Search phase.

7. (*Previously presented*) A content addressable memory according to claim **1** including a return line from the end of the chain of cells back to the CAM control unit for changing state in response to all Match flip-flops in the chain having been accessed.

8. (*Previously presented*) A method of operating a wherein] comprising the steps of choosing a standard byte address in all data blocks and including a byte different from the inactive state of the data bus in that address in every data block.

9. (*Previously presented*) A method of operating a content addressable memory according to claim **1** wherein each cell is divided into a plurality of distinct data blocks.

10. (*Previously presented*) A method of operating a content addressable memory according to claim **1** wherein a plurality of cells are combined into an extended data block with all cells of the block including corresponding key fields.

11. (*Previously presented*) A method of operating a content addressable memory according to claim **1** further including choosing a standard byte address in all data blocks and filling the data blocks with one data value if the data block in that cell is valid and another data value if the data block in the cell is cleared.

12. *Cancelled*